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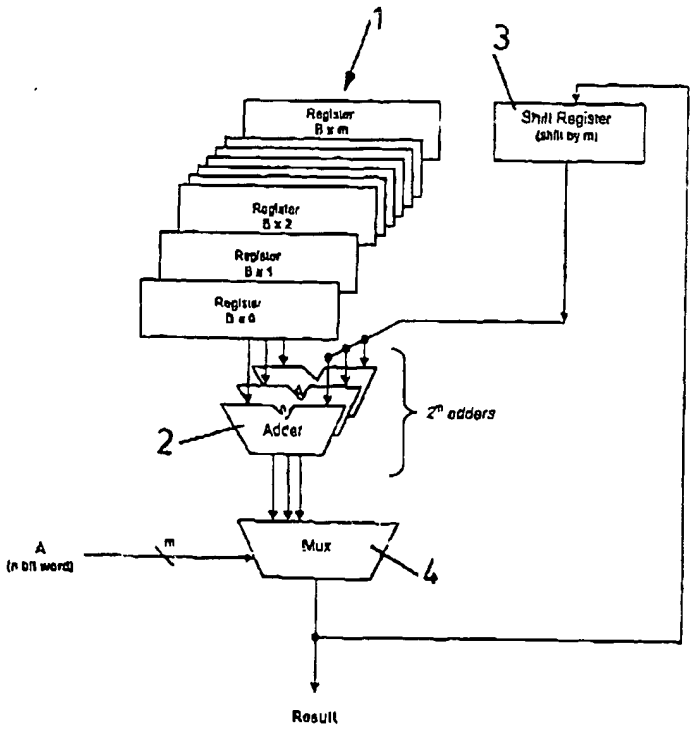
(54) Title: A SERIAL–PARALLEL BINARY MULTIPLIER

(57) Abstract

A serial binary multiplier multiplies two operands to provide a product. A first operand is stored locally and a second operand is transmitted serially whilst simultaneously multiplying said first operand with all possible values of said second operand taking into account any received bits of the second operand. All possible results are added to the contents of a partial result register and stored and when a complete element of the full second operand has been received and decoded, the correct result is selected by the decoder. The new partial product is shifted in the register and when all the bits of the second operand have been received the final product is output to a serial to parallel converter. The method and circuit permit part of the multiplication process to be performed whilst the input data is still being transmitted thereby reducing the operation delay. In a 1–bit two's complement embodiment a decoder is used to decide whether to add or substract the received bit of the serially transmitted operand to or from the contents of the partial result register. The decoder uses knowledge of the previously transmitted bit of the operand to make this decision.



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A SERIAL BINARY MULTIPLIER

The present invention relates to a serial binary multiplier for performing fixed point multiplication in data processing apparatus.

Central processing units of data processing apparatus generally incorporate a multiplier unit for performing multiplication operations. Typically such multiplier units are based on well known array multiplier designs or a shift-and-add algorithm. Multiplier units of this kind are generally optimised for performance (i.e. processing power and speed) or for compact implementation.

One example of a multiplier unit having compact size is described in our co-pending international patent application No. GB97/01520.

However, the performance of a serial multiplier, unlike an array multiplier design, is dependent on the total transmission delay in performing a sequence of operations as the serial data is received. The total transmission delay is a combination of several delays in the sequential operation of the multiplication process, namely: a delay as the data is routed to the input of the multiplier; a delay as the data passes through the interconnect; and the multiplier operation delay.

In monolithic design circuit performance has improved many fold as semiconductor processing techniques have lead to smaller and smaller component geometries. Contemporary integrated circuit process technology enables the manufacture of deep sub-micron circuit elements with physical dimensions of less than one micron. The performance of these circuits is often no longer determined by the operation of the active circuit components but is dominated by the interconnect delay between them.

The difference between the performance of active components, for example transistors, and the interconnect, or routing, is greatly exaggerated in the implementation of programmable circuits such as Field Programmable Gate Arrays (FPGAs), where greater flexibility in the interconnect structures adds further to the delay imposed on signals passing through them.

An alternative known approach to constructing a high performance multiplier is to base the design around a look-up-table. This is demonstrated in Altera's FLEX

10K device. Using this technique all the possible results of the multiplication process are stored in a table and the input operands are used to choose one result from the table. The size of such multipliers becomes very large when, say, operands of 8 bits or more are used. The multiplication of n-bit wide operands requires a table with 2^{2n} entries. An improvement to this design is to use multiple smaller look-up tables followed by a calculation step. This technique is also shown in Altera's FLEX 10K device. The latter technique reduces the size of the multiplier but degrades the performance since a further calculation step is required after a preliminary result has been selected from the look-up table.

It is an object of the present invention to obviate or mitigate the aforesaid disadvantages and to improve the performance of the data processing function of multiplication.

According to a first aspect of the present invention there is provided a serial binary multiplier for multiplying two binary operands to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving elements of a second operand serially, a calculation unit for calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, said possible results being calculated during transmission of the second operand, means for selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

By using the calculation unit to calculate partial products whilst the second operand is transmitted the delay in transmitting the data is less significant in the overall time required to conduct the multiplication process.

Preferably the second operand comprises a plurality of elements each comprising an m-bit word. In an embodiment where m=1 the calculation unit is an adder.

The calculation unit calculates all possible results on the basis of the value of the first operand and the value of previously received elements of the second operand.

The means to output the contents of the register preferably provides the final result in serial form.

In one preferred embodiment the first and second operands and the final product are in two's complement form and the possible results are calculated from the first operand, the partial product and the previously received bit of the second operand. In such an embodiment the calculation unit is an adder and subtractor and may take the form of a single circuit capable of addition and subtraction, the operation being determined by the value of the previously received bit.

According to a second aspect of the present invention there is provided a method of operating a serial binary multiplier for multiplying two binary operands to provide a product comprising the steps of storing a first operand, storing a partial product in a register, transmitting elements of a second operand serially whilst simultaneously calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

Specific embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a block diagram of an embodiment of an m-bit binary serial multiplier according to a first embodiment of the present invention;

Figure 2 is a block diagram of an embodiment of a 1-bit binary multiplier according to a second embodiment of the present invention;

Figure 3 is a block diagram of the multiplier of figure 2 adapted for two's complement operation according to a third embodiment of the present invention;

Figure 4 is a table showing the calculation process of the multiplier shown in figure 3; and

Figure 5 is a timing diagram for a single cycle of the multiplier operation.

Referring now to the drawings, figure 1 shows the structure of an m-bit serial multiplier which performs the multiplication operation on a locally stored first operand B and a second operand A that is transmitted to multiplier in the form of a serial stream of m-bit wide data elements, the m bits of each data element being received in parallel and multiple serial data elements forming the complete operand data word.

The multiplication process is performed by a calculation unit that comprises a bank of 2^m registers 1 and a bank of 2^m adders 2. The registers 1 store all possible 2^m results of multiplying the first operand B with all possible (2^m) values of the second operand A. Each register 1 within the bank stores one result of multiplying the first operand B with an assumed value of the second operand A. Each of these 2^m multiplication results is passed to one of the adders 2 in the bank of 2^m adders where it is summed with a partial product of the overall multiplication process that is stored in a shift register 3. The results of the addition process are then passed to a multiplexer 4.

A decoder (not shown) receives the m-bit serial input data element of the second operand A and on the basis of this, selects the appropriate correct result via the multiplexer 4. Thus the input data is used to select a pre-calculated result late in the calculation process. The selected (partial) result is then stored in the shift register 3 which reformats the partial result by shifting the stored data by m-bits to the right. The partial result is then recirculated to the input of the bank of adders 2. The multiplication process described above is then repeated for the next received data element of the second operand A until the whole of the input data word of the second operand A has been received and processed. If the input data represents the value zero then the recirculated output of the shift register can simply added to the register 3 rather than selecting the appropriate adder output. The final result in the shift register 3 is transmitted to a parallel to m-bit serial converter (not shown) which outputs the final result (product) in the original m-bit serial format.

The above described multiplier allows the parallel operation of both the multiplier operation (including addition of the products to the partial result in the shift register 3) and the input data transmission. Using a locally stored first operand B a number of possible multiplier results is pre-calculated independently of the second operand A and added to the partial result from the previous cycle. In this way the multiplication process delay and the data transmission delay occur simultaneously, or in parallel. The second operand A is only needed to complete the multiplication process by selecting one of the pre-calculated results. By employing a decoder that selects the appropriate partial result the delay generally associated with the multiplication process is reduced, whilst avoiding the need for a large look-up table of possible results.

It will be appreciated that by using the locally stored first operand B in the preliminary multiplication process, the number of possible pre-calculated results is greatly reduced in comparison to conventional multipliers based on look-up table designs.

Figure 2 shows an embodiment of the present invention that is used to multiply 1-bit serial input data. A 1-bit serial multiplier is highly suited to realisation within a programmable device, since implementing programmable interconnects between functional units that only require a single point-to-point connection is both practical and well known.

The operation of the 1-bit multiplier is similar to that of the generic m-bit multiplier example described earlier, however, using a 1-bit wide input format allows a novel optimisation of the circuit.

Since the input data of the second operand must be either a 1 or a 0 then only one dynamic calculation is required as there are only 2 possible results, one of which is a null operation (i.e. multiplication by zero). The structure of the 1-bit multiplier varies from the m-bit multiplier in that the calculation unit only comprises a single register to store the first operand B and a single adder. Parts corresponding to those of figure 1 are indicated by the same reference numerals increased by 100 and are not further described except insofar as they differ from their counterparts in figure 1.

The calculation unit 1, 2 shown in Figure 1 can be constructed in the 1-bit multiplier embodiment of figure 2 by using a register store for operand B and a single adder 102. The implementation of such a circuit is well known. When the multiplication operation is initiated the previous serial input bit is taken to be a zero. Once the current signal data input bit of the second operand A has been received it is used to determine whether the selected result is to be the result dynamically calculated by the adder (the sum of the received bit of the second operand A and the partial product in the register 103) or the previous partial result (i.e. no operation is performed). The final result is output via a parallel to serial converter 105.

Figure 3 shows a multiplier design for multiplication of 1-bit operands in two's complement format. The serially transmitted second operand A is decoded by a decoder 207 and the output provides instructions to an adder/subtractor 208 to choose the dynamic calculation operation i.e. either to add or to subtract the local operand B to or from the partial result that is fed back from the shift register 203. These add and subtract instructions are decoded from the previous signal data input bit and allow the dynamic calculation to be performed in parallel with the current signal data bit being transmitted. When the multiplication operation is initiated the previous serial input bit is taken to be a zero. Once the current signal data bit has been received and decoded it is used to determine whether the selected result is to be the result dynamically calculated by the multiplier or the previous partial result (i.e. no operation is performed) according to the table shown in figure 4.

The timing diagram for a single cycle of the 1-bit two's complement multiplier operation is shown in Figure 5. The opening part of the clock cycle is available for the independent dynamic calculation of partial result(s) on the basis of the previously received data bit, and for the transmission of the current data bit. This is shown as "Tmult" in Figure 4. The remaining part of the clock cycle is then dedicated to the late select process that requires simple decoding of the current serial input data bit, which may be easily constructed with simple logic gates to give very high performance. The delay attributed to this process is shown as "Tselect" in Figure 4. Clearly, overlapping the data transmission delay and the multiplier operation delay in this late select

multiplier design offers greatly improved performance over traditional serial multipliers.

It will be appreciated that numerous modifications to the above described design may be made without departing from the scope of the invention as defined in the appended claims. For example, the shifting of the partial product stored in the shift register 3, 103, 203 may be performed by any equivalent operation such as modifying the connections to the register. The term "shifting" is used in the claims with the intention of incorporating such equivalent operations.

CLAIMS

1. A serial binary multiplier for multiplying two binary operands to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving elements of a second operand serially, a calculation unit for calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, said possible results being calculated during transmission of the second operand, means for selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

2. A serial binary multiplier according to claim 1, wherein the elements of the second operand are m-bit words.

3. A serial binary multiplier according to claim 2, wherein m=1 and the calculation unit is an adder.

4. A serial binary multiplier according to claim 1, 2 or 3, wherein the calculation unit calculates all possible results on the basis of the value of the first operand and the value of previously received elements of the second operand.

5. A serial binary multiplier according to any preceding claim, wherein the means to output the contents of the register provides the final result in serial form.

6. A serial binary multiplier according to any preceding claim, wherein the first and second operands and the final product are in two's complement form and the

possible results are calculated from the first operand, the partial product and the previously received bit of the second operand.

7. A serial binary multiplier according to claim 6, wherein the calculation unit is an adder and subtractor.

8. A serial binary multiplier according to claim 7, wherein the calculation unit is a single circuit capable of addition and subtraction, the operation being determined by the value of the previously received bit.

9. A method of operating a serial binary multiplier for multiplying two binary operands to provide a product comprising the steps of storing a first operand, storing a partial product in a register, transmitting elements of a second operand serially whilst simultaneously calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

10. A serial binary multiplier substantially as hereinbefore described with reference to the accompanying drawings.

11. A method of operating a serial binary multiplier substantially as hereinbefore described with reference to the accompanying drawings.

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WO 00/34853 PCT/GB99/03897

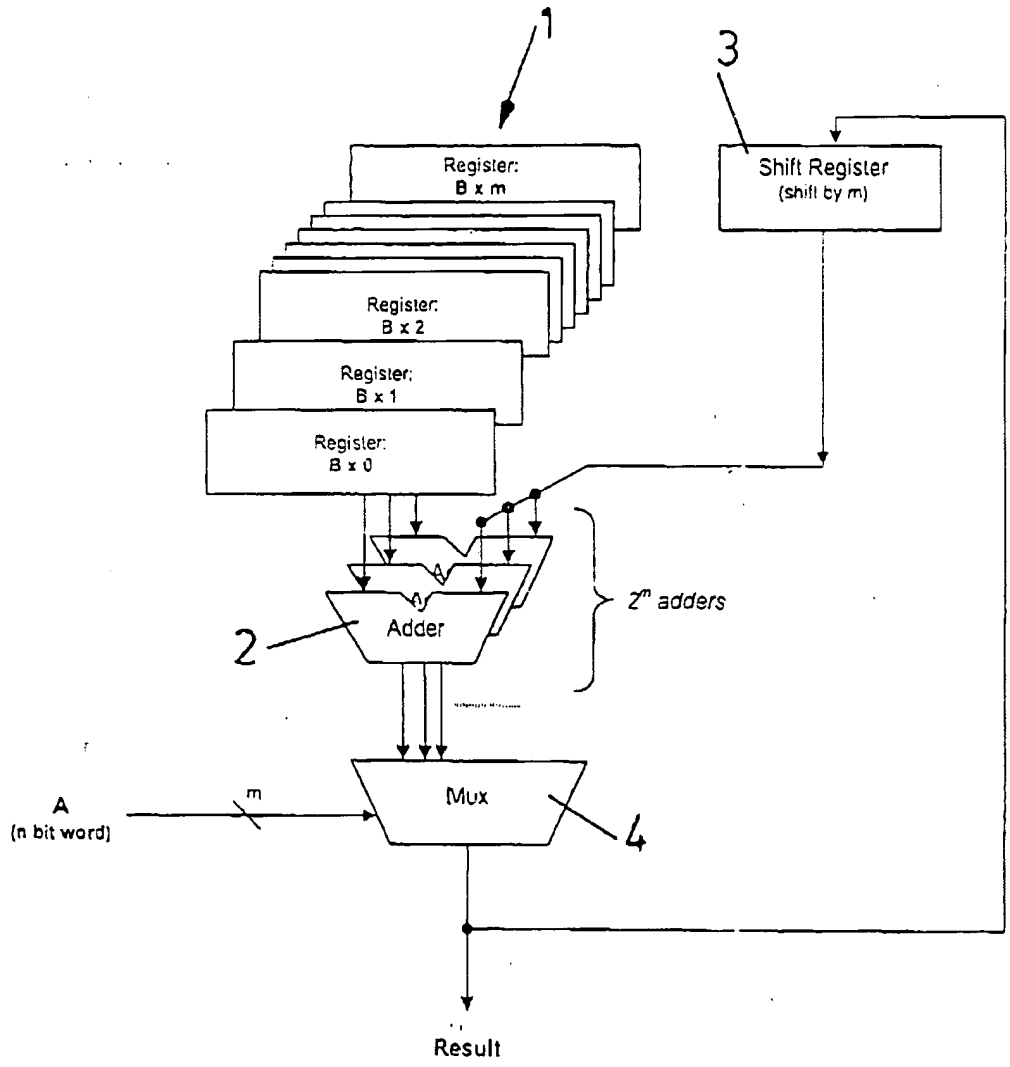
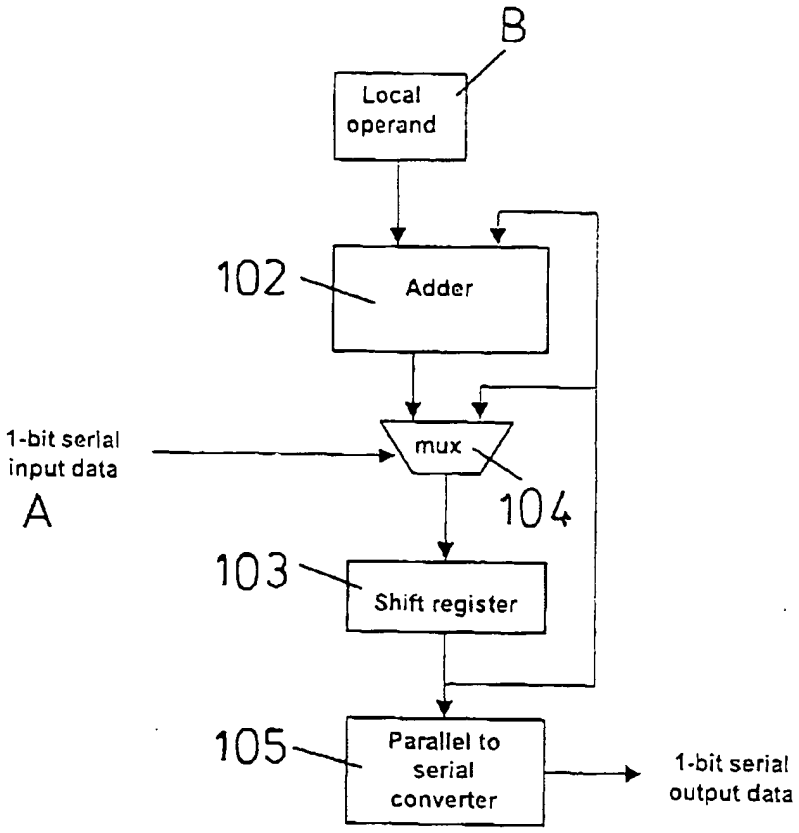


FIG. 1


B
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102
Adder
1-bit serial input data
A
mux
104
103
Shift register
105
Parallel to serial converter
1-bit serial output data

FIG. 2

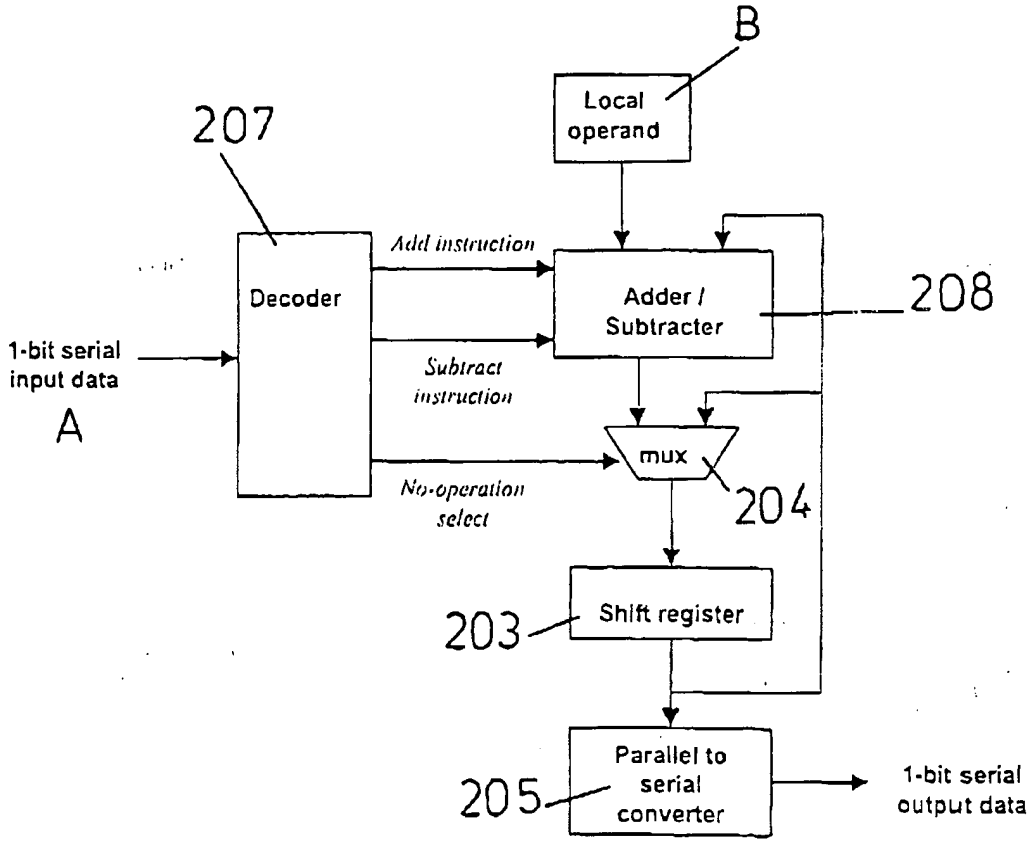
B
Local operand
207
Decoder
Add instruction
Adder / Subtracter
208
1-bit serial input data
A
Subtract instruction
mux
No-operation select
204
203
Shift register
Parallel to serial converter
205
1-bit serial output data

FIG. 3

Current serial input bit	Previous serial input bit (or 0 in first instance)	Pre-calculation	Selected result
0	0	Subtract local operand from partial result	No operation
1	0	Subtract local operand from partial result	Pre-calculated result
1	1	Add local operand to partial result	No operation
0	1	Add local operand to partial result	Pre-calculated result

FIG. 4

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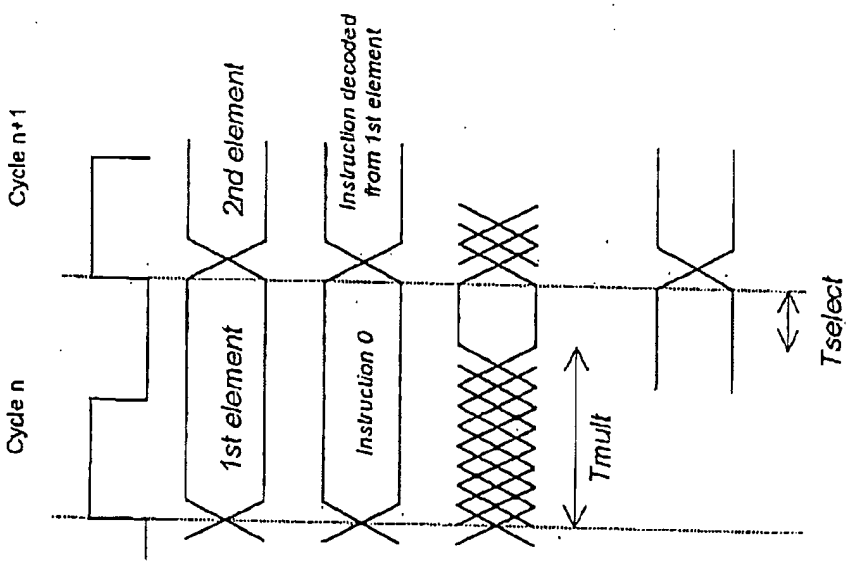

FIG. 5

PATENT COOPERATION TREATY

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
DE/J088294PWO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/GB 99/ 03897	24/11/1999	04/12/1998
Applicant		
SYSTOLIX LIMITED et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

   [ ] the text is approved as submitted by the applicant.

   [X] the text has been established by this Authority to read as follows:

   A SERIAL-PARALLEL BINARY MULTIPLIER

5. With regard to the **abstract**,

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 1

   [ ] as suggested by the applicant.

   [X] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/03897

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F7/52

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 539 685 A (OTAGURO YUKIO) 23 July 1996 (1996-07-23) figure 1	1-11
X	S. SKLAR: "2's complement Arithmetic Operations" COMPUTER DESIGN., vol. 11, no. 5, May 1972 (1972-05), pages 115-121, XP002130443 PENNWELL PUBL. LITTLETON, MASSACHUSETTS., US ISSN: 0010-4566 figures 3,4	8

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 February 2000	28/02/2000

Name and mailing address of the ISA	Authorized officer
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2

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 322 (P-1239), 16 August 1991 (1991-08-16) & JP 03 116327 A (TOSHIBA CORP;OTHERS: 01), 17 May 1991 (1991-05-17) abstract; figure	1,9
A	US 4 849 921 A (YASUMOTO MASAAKI ET AL) 18 July 1989 (1989-07-18) figure 1	1,9

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter[illegible]nal Application No
PCT/GB 99/03897

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5539685 A	23-07-1996	JP 6067851 A	11-03-1994
JP 03116327 A	17-05-1991	NONE	
US 4849921 A	18-07-1989	JP 61290534 A	20-12-1986
		JP 61296427 A	27-12-1986
		JP 62127940 A	10-06-1987
		CA 1257003 A	04-07-1989
		EP 0208939 A	21-01-1987

10K device. Using this technique all the possible results of the multiplication process are stored in a table and the input operands are used to choose one result from the table. The size of such multipliers becomes very large when, say, operands of 8 bits or more are used. The multiplication of n-bit wide operands requires a table with 2^{2n} entries. An improvement to this design is to use multiple smaller look-up tables followed by a calculation step. This technique is also shown in Altera's FLEX 10K device. The latter technique reduces the size of the multiplier but degrades the performance since a further calculation step is required after a preliminary result has been selected from the look-up table.

It is an object of the present invention to obviate or mitigate the aforesaid disadvantages and to improve the performance of the data processing function of multiplication.

According to a first aspect of the present invention there is provided a serial binary multiplier for multiplying two binary operands to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving elements of a second operand serially, a calculation unit for calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, said possible results being calculated during transmission of the second operand, means for selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

By using the calculation unit to calculate partial products whilst the second operand is transmitted the delay in transmitting the data is less significant in the overall time required to conduct the multiplication process.

Preferably the second operand comprises a plurality of elements each comprising an m-bit word. In an embodiment where m=1 the calculation unit is an adder.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
DE/J088294PWO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/03897	24/11/1999	04/12/1998
International Patent Classification (IPC) or national classification and IPC G06F7/52		
Applicant SYSTOLIX LIMITED et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 2 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
05/06/2000	17.11.2000
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Nussbaumer, C Telephone No. +49 89 2399 2145

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/03897

I. Basis of the r port

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1,3-7	as originally filed			
2,2a	as received on	01/11/2000	with letter of	01/11/2000

Claims, No.:

1-11	as originally filed

Drawings, sheets:

1/5-5/5	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

- ☐ the entire international application.
- ☒ claims Nos. 10,11.

because:

- ☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (*specify*):
- ☒ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. 10,11 are so unclear that no meaningful opinion could be formed (*specify*):
  see separate sheet
- ☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.
- ☐ no international search report has been established for the said claims Nos. .

2. A meaningful international preliminary examination report cannot be carried out due to the failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

- ☐ the written form has not been furnished or does not comply with the standard.
- ☐ the computer readable form has not been furnished or does not comply with the standard.

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	5-8
	No:	Claims	1-4,9
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-9
Industrial applicability (IA)	Yes:	Claims	1-8
	No:	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

Reference is made to the following documents:

D1: US-A-5 539685 [TOSHIBA];

D2: S. SKLAR: '2's complement Arithmetic Operations' COMPUTER DESIGN., vol. 11, no. 5, May 1972 (1972-05), pages 115-121, XP002130443 PENNWELL PUBL. LITTLETON, MASSACHUSETTS., US ISSN: 0010-4566.

Re Item III

Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. Claims 10 and 11 are not clear in the sense of Article 6 PCT for the reasons set out in the Gazette of PCT, Preliminary Examination Guidelines according to the PCT, Section, IV, Chapter III 4.10.

Re Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Claims 1 to 4 and 9 do not appear to be new in sense of Article 33 (2) PCT.

1.1 D1 discloses a serial multiplier (see D1, column 1, lines 15-42; figure 1 falling under the terms of claim 1 as long as m is not defined. In D1, m is equal to 1. Figure 1 of D1 is self explanatory when making correspondences with the features of claim 1 (or claim 9). The main aspect being the calculation unit (made of the ADDER 4 combined with the connection line bringing Z<0:3> to selector 5) preparing all the possible results, in that case the two possible results 0xY+partial product and 1xY+partial product for being selected based on the serially received element one bit of the operand stored in X, and these possible results being calculated during transmission of the multiplier (second operand).

1.2 The features of dependent claims 2 to 4 could also be identified in D1.

2. Dependent claims 5 to 8 do not appear to add any technical features to any claim they depend to in order to render the subject matter of the combination inventive in the sense of (Article 33(3) PCT) over the available prior art.

2.1 Providing a serialiser at the output of the multiplier is considered as a juxtaposition of technical features which does not lead to any inventiveness. This is furthermore in accordance with circumstances, that is the environment into which the multiplier is implemented in.

2.2 The features of claims 6 to 8 have already been employed for the same purpose in a similar multiplier, see document D2, page 117, section entitled "Multiplication". It would be obvious to the person skilled in the art, namely when the same result is to be achieved, to apply these features with corresponding effect to a multiplier according to document D1, thereby arriving at a multiplier according to claims 6 to 8.

Re Item VII

Certain defects in the international application

1. The requirements of Rule 6.2(b) PCT, the features of the claims being provided with reference signs placed in parentheses, is not satisfied.

2. The description on page 1, lines 8-9 does not refer to a document which are available to the public and which can be easily retrieved (cf. Gazette of PCT, Preliminary Examination Guidelines according to the PCT, section IV, chapter II, 4.18).